AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method of placing a circuit design comprising a component having input signals with asymmetric delays, the method comprising [[the]] steps of:

first identifying topological levels of the circuit design;

determining an arrival time for each input signal of a plurality of input signals to the component ;

identifying a propagation delay associated with each input port of a plurality of input ports of the component ; and

ordering the plurality of input signals of the component according to [[the]] arrival times associated with the plurality of input signals and [[the]] propagation delays associated with the plurality of input ports of the component.

Claim 2. (Cancelled)

3. (Currently Amended) The method of claim [[2]] 1, further comprising repeating said determining, said identifying, and said ordering steps for each component within [[an]] one of said identified topological levels.

4. (Currently Amended) The method of claim 3, further comprising iteratively performing said repeating step for each of said identified topological levels of the circuit design.

5. (Currently Amended) The method of claim 4, wherein the identified topological levels are processed in hierarchical order.

6. (Original) The method of claim 5, further comprising updating timing information for the circuit design after ordering input signals of each component of an identified topological level.

7. (Currently Amended) The method of claim 1, said ordering step further comprising [[the]] a step of matching input signals having an earlier arrival time with input ports of the component having longer propagation delays.

8. (Currently Amended) The method of claim 7, wherein said matching step matches a first input signal having [[an]] the earliest arrival time with a first input port of the component having [[a]] the longest propagation delay, and a second input signal having [[a]]the latest arrival time with an input port of the component having [[a]] the shortest propagation delay.

9. (Currently Amended) The method of claim 1, said ordering step comprising:

sorting input signals according to an arrival time at the component;

sorting input ports of the component according to propagation delay; and

matching said sorted input signals having an earlier arrival time with said sorted input ports ~~of the component~~ having longer propagation delays.

10. (Currently Amended) The method of claim 9, wherein said matching step matches an input signal having [[an]] the earliest arrival time with an input port of the component having [[a]] the longest propagation delay, and an input signal having [[a]] the latest arrival time with an input port of the component having [[a]] the shortest propagation delay.

11. (Original) The method of claim 1 wherein the component is a look-up table (LUT).

12. (Currently Amended) A system for placing a circuit design comprising:

means for first identifying topological levels of the circuit design;

means for determining an arrival time for each input signal to a component within a circuit design representation;

means for identifying [[the]] propagation delay associated with each pin of the component; and

means for ordering input signals of the component according to the arrival time[[s]] of each input signal and the propagation delay of each pin of the component; and

means for causing said means for determining, said means for identifying, and said means for ordering to operate on each component within an identified topological level.

13. (Original) The system of claim 12, wherein the component is a look up table.

Claim 14. (Cancelled)

15. (Currently Amended) The system of claim [[13]] 12, further comprising means for iteratively processing each of identified topological levels of the circuit design representation, wherein said means for iteratively processing processes the topological levels in hierarchical order.

16. (Original) The system of claim 15, further comprising means for updating timing information for the circuit design representation after ordering input signals of each component of an identified topological level.

17. (Original) The system of claim 12, said means for ordering further comprising means for matching input signals having an earlier arrival time with pins of the component having longer propagation delays.

18. (Currently Amended) The system of claim 17, wherein said means for matching matches an input signal having [[an]] the earliest arrival time with a pin of the component having [[a]] the longest propagation delay, and an input signal having [[a]] the latest arrival time with a pin of the component having [[a]] the shortest propagation delay.

19. (Original) The system of claim 12, said means for ordering further comprising:

means for sorting input signals according to an arrival time at the component;

means for sorting pins of the component according to propagation delay; and

means for matching input signals having an earlier arrival time with pins of the component having longer propagation delays.

20. (Currently Amended) The system of claim 19, wherein said means for matching matches an input signal having [[an]] the earliest arrival time with a pin of the component having [[a]] the longest propagation delay, and an input signal having [[a]] the latest arrival time with a pin of the component having [[a]] the shortest propagation delay.

21. (Currently Amended) A machine readable storage, having stored thereon a computer program having a plurality of code sections executable by a machine for causing the machine to perform [[the]] steps of:

determining an arrival time for each input signal to a look up table within a circuit design representation;

identifying [[the]] propagation delay associated with each pin of the look up table; and

ordering input signals of the ~~lookup~~ look up table according to the arrival time[[s]] of each input signal and the propagation delay of each pin of the look up table.

22. (Currently Amended) The ~~machine readable storage~~ the computer program of claim 21, further causing the machine to perform [[the]] a step of first identifying topological levels of the circuit design representation.

23. (Currently Amended) The ~~machine readable storage~~ the computer program of claim 22, further causing the machine to perform [[the]] a step of repeating said determining, said identifying, and said ordering steps for each look up table within an identified topological level.

24. (Currently Amended) The ~~machine readable storage~~ the computer program of claim 23, further causing the machine to perform [[the]] a step of iteratively performing said repeating step for each identified topological level of the circuit design representation.

25. (Currently Amended) The ~~machine readable storage~~ the computer program of claim 24, wherein the identified topological levels are processed in hierarchical order.

26. (Currently Amended) The ~~machine readable storage~~ the computer program of claim 25, further causing the machine to perform [[the]] a step of updating timing information for the circuit design representation after ordering input signals of each look up table of an identified topological level.

27. (Currently Amended) The ~~machine readable storage~~ the computer program of claim 21, wherein said ordering step further comprising [[the]] a step of matching input signals having an earlier arrival time with pins of the lookup table having longer propagation delays.

28. (Currently Amended) The ~~machine readable storage~~ the computer program of claim 27, wherein said matching step matches an input signal having an earliest arrival time with a pin of the [[lookup]] look up table having a longest propagation delay, and an input signal having a latest arrival time with a pin of the [[lookup]] look up table having a shortest propagation delay.

29. (Currently Amended) The ~~machine readable storage~~ the computer program of claim 21, wherein said ordering step comprising:

sorting input signals according to an arrival time at the look up table;

sorting pins of the look up table according to propagation delay; and

matching input signals having an earlier arrival time with pins of the look up table having longer propagation delays.

30. (Currently Amended) The ~~machine readable storage~~ the computer program of claim 29, wherein said matching step matches an input signal having [[an]] earliest arrival time with a pin of the lookup table having [[a]] the longest propagation delay, and [[an]] the input signal having [[a]] the latest arrival time with a pin of the lookup table having [[a]] the shortest propagation delay.